AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 20. (canceled)

21. (new) A signal processing integrated circuit comprising a plurality of channels comprising a plurality inputs coupled to plurality of amplifiers, wherein the amplifiers amplify any signals coming to the plurality of inputs, each input amplifier is part of a channel of said plurality, said readout channels comprising:

a means for receiving one or more input signals;

an amplifier coupled to said input for integrating said one or more input signals and outputting an amplified signal;

a processing circuit for processing the said amplifier output, and

a means for outputting said processed signals responsive to said input signals.

22. (new) The integrated circuit channel of claim 21, wherein a polarity switching circuit is included.

23. (new) The integrated circuit channel of claim 22, wherein said polarity switching circuit is externally controlled.

24. (new) The integrated circuit channel of claim 21, further comprising a gain stage coupled to said charge sensitive amplifier.

25. (new) The integrated circuit channel of claim 21, further comprising a shaper amplifier for providing shaped, integrated detector signals responsive to said selected signal.

26. (new) The integrated circuit channel of claim 25, wherein said shaped, integrated detector signal is of an approximately inverted bell shaped form.

27. (new) The integrated circuit channel of claim 25, wherein said shaped, integrated detector signal is of an approximate uninverted bell shaped form.

28. (new) The integrated circuit channel of claim 21, further comprising a peak hold or sample and hold circuit coupled to output of the said amplifier.

29. (new) The integrated circuit channel of claim 21, further comprising a plurality of comparators.

30. (new) The integrated circuit channel of claim 29, wherein the comparators can be a leading edge, a zero crossing or a constant fraction type or a mixture of such comparators.

31. (new) The integrated circuit channel of claim 29, wherein said plurality of comparators enclose at least one predetermined energy band.

32. (new) The integrated circuit channel of claim 30, further comprising a differentiator circuit coupled to at least one of said first plurality of comparators, said differentiator circuit producing a fast trigger output with low jitter.

33. (new) The integrated circuit channel of claim 28, wherein an output of said peak hold circuit is multiplexed to said means for outputting.

34. (new) The integrated circuit channel of claim 29, wherein an output of at least one of said plurality of comparators initiates a readout cycle of said data readout integrated circuit.

35. (new) The integrated circuit channel of claim 21, wherein said data outputting means outputs a readout signal for at least one channel of said plurality of integrated circuit channels

containing an input signal.

36. (new) The integrated circuit channel of claim 35, wherein said data outputting means only outputs said readout signal for said channel of said plurality of integrated circuit channels for which a said trigger signal has been received.

37. (new) The integrated circuit channel of claim 35, wherein said data outputting means outputs said readout signal for said channel of said plurality of integrated circuit channels after said trigger signal has been received for any one of said plurality of integrated circuit channels.

38. (new) The integrated circuit channel of claim 37, wherein said trigger signal is an external trigger signal.

39. (new) The integrated circuit channel of claim 21, wherein said data outputting means outputs a readout signal for one triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay between said readout signal and said disablement of said remaining channels is controlled by an externally supplied signal.

40. (new) The integrated circuit channel of claim 21, wherein the

said amplifier is charge sensitive type.

41. (new) The integrated circuit channel of claim 21, wherein the said amplifier changes the signal into a voltage output type.

42. (new) The integrated circuit channel of claim 40, wherein said input charge sensitive amplifier has an active or passive resistive feedback circuit.

43. (new) The integrated circuit channel of claim 21, wherein the said amplifier is a current integrating type.

44. (new) The integrated circuit channel of claim 29, further comprising a first comparator of said plurality of comparators is a low level discriminator, and

wherein at least one of said first comparator allows an output trigger when a peak hold circuit output is larger than a first threshold voltage.

45. (new) The integrated circuit channel of claim 29, further comprising a second comparator of said plurality of comparators wherein said second comparator is an upper level discriminator, and

wherein said second comparator only issues a signal when said peak hold circuit output is larger than a second threshold

voltage.

46. (new) The integrated circuit channel of claim 21, further comprising circuitry for measuring time difference of said input signals between different channels.

47. (new) The integrated circuit of claim 21 includes a control and setting circuit.

48. (new) The integrated circuit channel of claim 29, wherein the plurality of comparators can be a single comparator.

49. (new) The integrated circuit channel of claim 29, wherein the plurality of comparators can be of discriminator type.

50. (new) The integrated circuit channel of claim 29, wherein the plurality of comparators may have at least one fast comparator.

51. (new) The integrated circuit channel of claim 35, wherein said data outputting means uses sparse readout capability.

52. (new) The integrated circuit channel of claim 51, wherein said sparse readout capability also includes means to readout other channels which may also have signal which has not produced a said trigger in that channel.

53. (new) The integrated circuit channel of claim 21, further comprising circuitry for pole zero cancellation.